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(71) Applicant
The Plessey Company plc

(Incorporated in United Kingdom)

Vicarage Lane, Ilford, Essex, IG1 4AQ

(72) Inventors
Anthony Peter Hulbert
Michael Richard Richardson

(74) Agent and/or Address for Service
F Elliott
The Plessey Company Plc
Intellectual Property Department, Vicarage Lane,
Ilford, Essex, IG1 4AQ

(54) Correlator for synchronisation detection

(57) The correlator is made up of a plurality of short correlators 20, each of which provides correlation of a reference synchronisation sequence, in one of a plurality of sampling phases, of an incoming sync word. To determine the optimum sampling phase, both the total correlation score C must exceed a given threshold from 32, and at least one of the short correlators must yield a correlation hit, D.

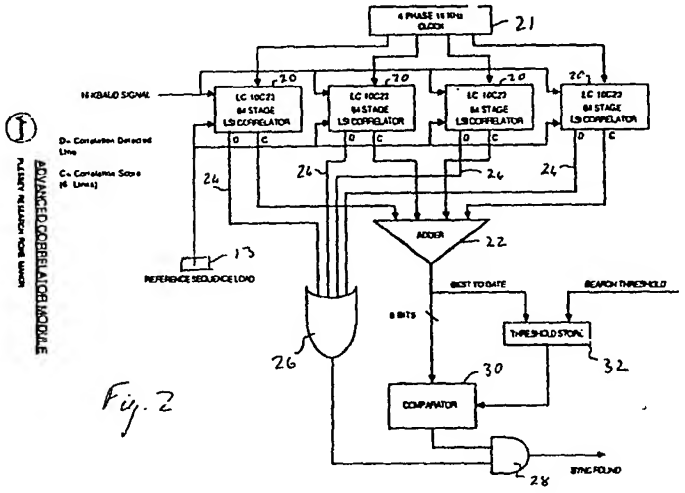

Fig. 2

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The claims were filed later than the filing date within the period prescribed by Rule 25 (1) of the Patents Rules 1982.

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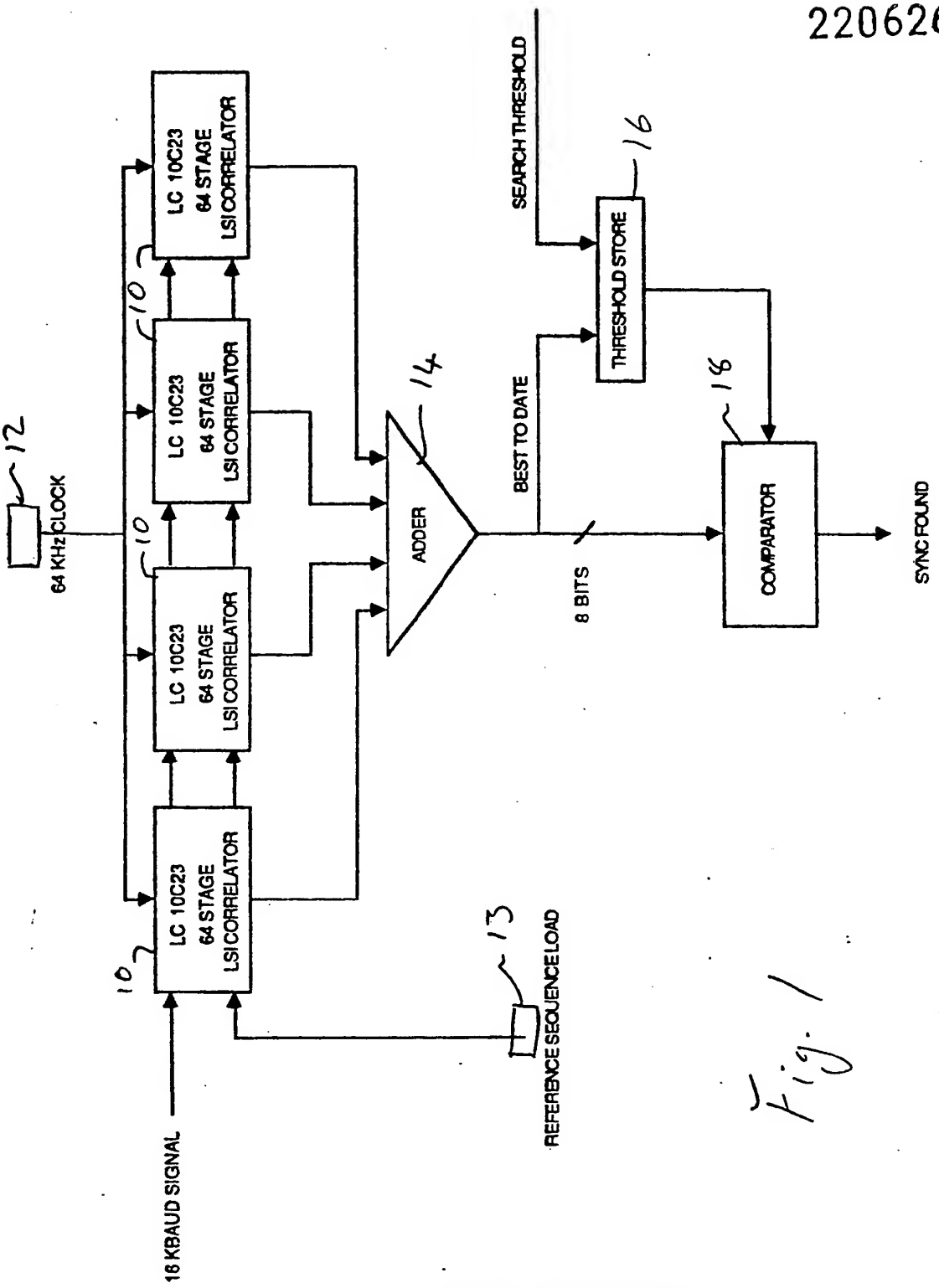

Fig. 1

CORRELATOR MODULE

PLESSEY RESEARCH ROKE MANOR

FIGURE

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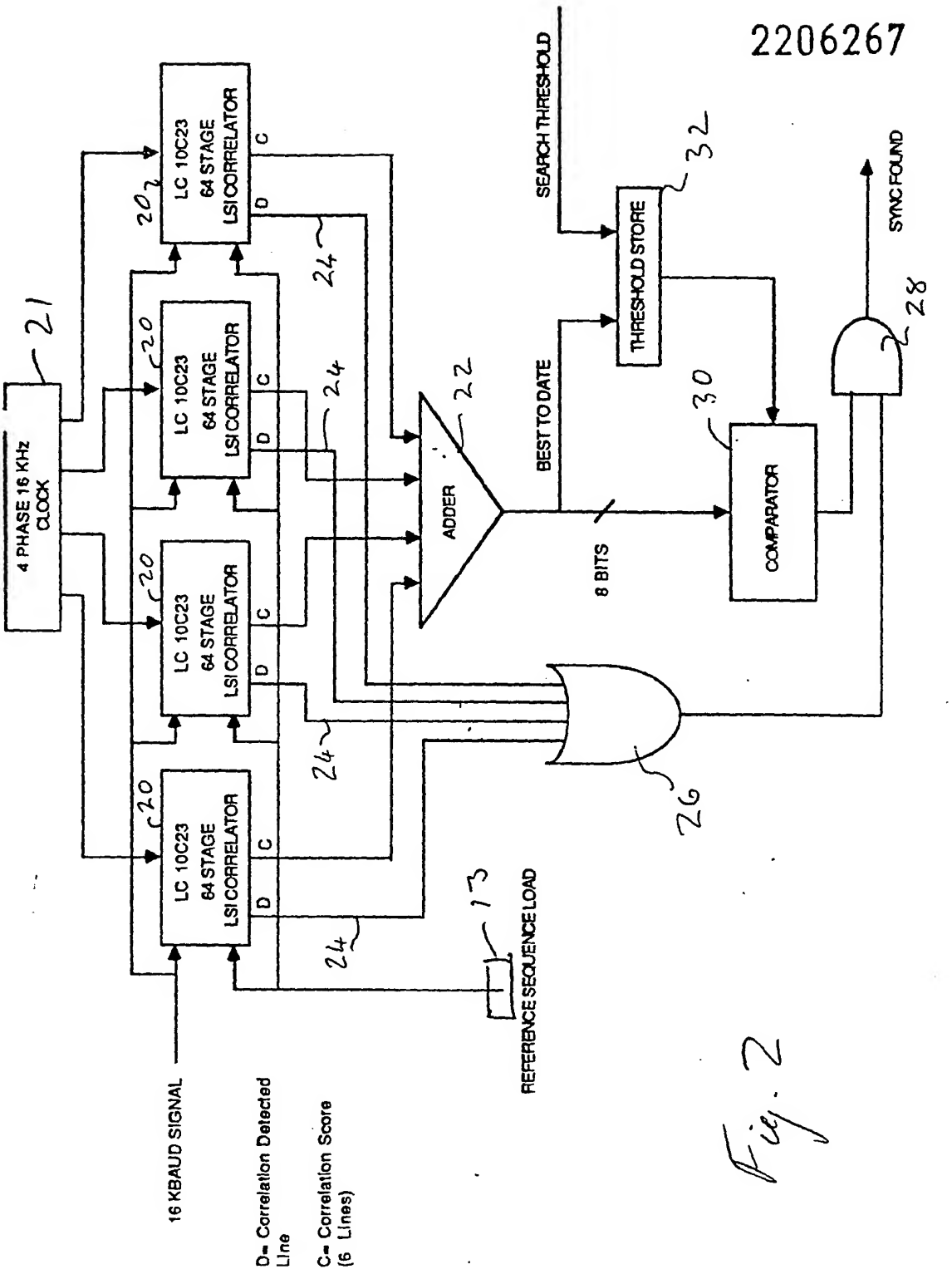

Fig. 2

ADVANCED CORRELATOR MODULE

PLESSEY RESEARCH ROKE MANOR

FIGURE

NOVEL CORRELATOR FOR SYNCHRONISATION DETECTION.

Synchronisation is employed, for example, in synchronous data transmission, to identify a signal and to resolve bit and frame timing. Synchronisation is commonly based upon the transmission of an n bit sync word. A correlator will operate upon the incoming received demodulated output, sampled at m times per bit. This will resolve bit timing to within $\pm 1/2m$ bits thereby maximising the overall demodulation performance. When the correlation exceeds a given threshold, the sync word will be deemed to be present. It is possible to perform the correlation in two different ways as follows:-

a) Over-sample the incoming received data in a bit ratio of m:1. This will produce a stream of data bits of length n X m in which, nominally, all bits in each group of m bits are the same. This is correlated against a (nominally) identical n X m bit sequence in which, again, each of the bits of the original n bit sequence is replicated m times. This will produce a correlation peak which is triangular about the nominal ideal sampling position and which is approximately ± 1 bit wide. The normal approach for the design of a long correlator where the total length m X n is greater than the length of any specific hardware correlator device available, is to string the correlators together such that each handles (n X m)/k bits where k is the total number of correlators used. The correlation sequence is divided between the correlators in sequence such that correlator 1 holds bits 1 to (n X m)/k, correlator

2, bits (n X m)k+1 to 2(n X m)/k etc. The scores of the k correlators are added to provide the total correlation score.

Figure 1 shows a typical long correlator. Four 64 bit correlators 10 are clocked at 64 kHz by a clock 12 at four times the incoming bit rate of 16 K Baud. A reference source 13 provides an n X m bit sequence identical to the sync word. Thus, if there are n bits in the synchronisation word, each bit is sampled m (four) times. As in this case, k is equal to four, the correlator is effectively a 256 bit correlator. The correlation score from each of the correlators 10 is summed in a four-input adder 14. The maximum output of the adder 14 is stored in a store 16 and this maximum is compared to the instantaneous value of the output of the adder 14 in a comparator 18 to give a "sync found" output. This approach is useful in that it readily emphasises the position of the optimum sampling point, both at low and high error rates. However, since the data is sampled arbitrarily, it is possible for a sampling error of up to $\pm 1/2m$ bits to arise. When this occurs, the correlation peak (in the absence of errors) is reduced to $(2m-1)/2m$ of its maximum value. In order to accommodate this condition in poor error conditions, it would be necessary to reduce the threshold below that which would otherwise be necessary. This could seriously degrade the false alarm performance.

b) The second manner of determining correlation uses m separate n bit correlators, each containing the nominal n bit sync word sequence. The incoming data is sampled m time per bit and commutates the samples to each of the m correlators in turn. For each of the correlators, the peak will be 1 bit wide. A timing error of $\pm 1/2m$ bits will not of itself reduce the correlation peak although non-optimum sampling of the demodulated signal will degrade the error performance of the link somewhat, thus reducing the correlation peak indirectly. Thus, this approach provides better sensitivity. However, at high signal-to-noise ratios at least m-1 correlators will provide an identical correlation peak and resolution of the ideal sampling phase will not be possible. It is quite possible that the error performance could degrade after reception of the sync word so optimum sampling is still a requirement even in this condition.

It is an object of the present invention to provide a method of and apparatus for synchronisation determination wherein the aforesaid disadvantages are minimised or overcome.

According to the present invention, there is provided a synchronisation correlator comprising m short correlators, each arranged to provide an output if its correlation threshold is exceeded, and a single n X m correlator to determine the optimum sampling phase. This would appear to require a complex circuit to achieve. This invention also provides a method of synchronisation correlation whereby the aforesaid combined approach can be

implemented without significant increase in complexity. It is actually possible to implement the synchronisation correlation with barely more complexity than a single long correlator circuit alone.

The invention will be described further, by way of example, with reference to Figure 2 of the accompanying drawings which shows, in block form, an improved correlator according to the present invention.

In our alternative approach, the correlators are used such that each handles successive bits of the original sync sequence rather than of the over-sampled sequence. This is applicable only where possible values of k are integer multiples of m (this is commonly the case and often k=m). Thus considering the over sampled sync word, correlators 1 to k/m will handle bits 1,m+1,2m+1,3m+1.....,(n-1)m+1, correlators k/m+1 to 2k/m will handles bits 2,m+2,2m+2,3m+2....,(n-1)m+2 and so on to correlators k-k/m+1 to k which will handle bits m,2m,3m,4m...,n X m. The scores of the k correlators are added together as for the other approach. However, in this approach, each set of k/m correlators provides the score to permit the short correlator results of 'b' above also to be obtained.

Our example is base upon n=64 and m=4 and k=4. Figure 2 shows an implementation of a combined correlator. In this implementation, each correlator 20 handles all 64 bits of the sync sequence from the incoming signal and also from the reference source 13 but the four correlators 20, are used so that each handles only one phase of a clock 21. For a long correlator, the sum of correlator outputs is applied an adder 22 but the individual correlators also provide threshold detection outputs 24, which are

used via OR gate 26 and AND gate 28, to gate the output of the long correlator from a comparator 30, which operates with a lower effective threshold.

As in the prior art (figure 1), a threshold store 32 is provided which stores the up-dated maximum output of the adder 22 and has a search threshold reference input. It will be seen that the additional complexity of the correlator of the invention is minimal; the use of a k phase clock, an OR gate and an AND gate, but the disadvantages of both types of prior art correlator are avoided whilst the advantages of both types are kept.

The invention is not confined to the precise details of the foregoing example and variations may be made thereto.

CLAIMS:

1. A synchronisation correlator for determining synchronisation of an n bit sync word comprising m short correlators each arranged to provide an output if its correlation threshold is exceeded, and a single n X m correlator to determine the optimum sampling phase.

2. A correlator as claimed in claim 1 wherein the m short correlators are each arranged to compare successive bits of an incoming sync word with corresponding bits of a reference sync word.

3. A correlator as claimed in claim 2 further including clock means having m phase output signals each short correlator being driven by a respective clock phase.

4. A correlator as claimed in claim 1, 2 or 3 wherein each short correlator provides a "score' output, the score outputs being summed in an adder and compared in a comparator with a threshold score obtained from a store.

5. A correlator as claimed in claim 4 wherein each short correlator provides a threshold detection output which outputs are OR-red and thereafter AND-ed with the output of the comparator.

6. A synchronisation correlator substantially as hereinbefore described with reference to and as illustrated in Figure 2 of the accompanying drawings.

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